

L Number	Hits	Search Text	DB	Time stamp
-	1	(arbitration with queue\$1 with (shar\$3 adj memory)) same cache	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 08:58
-	0	mem. adj int.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 08:58
-	163	xio	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 08:58
-	13	xio and multiprocess\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 08:58
-	17	silicon.as. and huffman.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 08:59
-	0	arbitration adj queue adj circuit	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:13
-	0	((arbit?r arbitration) with (queue adj circuit)) same cache	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:13
-	109	arbitration adj queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:13
-	8	(arbitration adj queue) same cache	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:15
-	0	collapsible adj3 queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:17
-	67891	collapsible	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:18
-	1	collapsible with queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:18
-	866	distributed adj shared adj memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:20

-	414	(distributed adj shared adj memory) same processor\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:21
-	14	(distributed adj shared adj memory) same processor\$1 same (memory adj interface)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:31
-	4	priority same (idle adj state) same win\$4 same busy	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:33
-	0	(hierarchical adj (mux multiplexer)) same priority	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:38
-	6	(hierarchical with (mux\$3 multiplexer\$3)) same priority	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 09:38
-	330	(arbitration arbit?r) adj3 queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 10:31
-	7545	collaps\$3 same (logic circuit mux\$3 multiplex\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 10:56
-	1	collaps\$3 same (logic circuit mux\$3 multiplex\$3) same 2:1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 10:56
-	28	collaps\$3 same (logic circuit mux\$3 multiplex\$3) same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 10:56
-	129	(queue fifo) same (updat\$3 adj3 (logic circuit))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 11:27
-	23262	(queue fifo) same (refresh\$3 (logic circuit))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 11:28
-	940	(queue fifo) same (refresh\$3 (logic circuit)) same idle	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 11:28
-	223	(queue fifo) with (refresh\$3 (logic circuit)) with idle	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 11:29

-	3	(queue fifo) with (refresh\$3 adj (logic circuit)) with idle	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 11:29
-	0	(queue\$3 adj\$3 operation) same enqueue same deque	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 13:36
-	21	enqueue same deque	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 13:51
-	559	(queue\$3 queue\$3) adj operation	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:10
-	25	((queue\$3 queue\$3) adj operation) same (mark\$3 idle)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:00
-	120	(mux\$3 multiplex\$3) same (fifo\$1 queue\$4) same (update\$3 refresh\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:01
-	584	(queue\$3 queue\$3) same (fragment\$5 defragment\$5 de-fragment\$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:10
-	128	(queue\$4 adj\$3 manage\$4) same (mux\$3 multiplex\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:18
-	139	queue same shift same (mux\$3 multiplex\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 14:45
-	73	(memory adj interface) same cache same (arbit?r (arbitration adj (logic circuit)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/01 16:29
-	28	compaction same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 08:13
-	0	initialize\$5 same idle same (all adj\$3 entries) same (queue adj location\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:02
-	0	initialize\$5 same idle same (all adj\$3 entries) same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:02

-	22	initializ\$5 same idle same entr\$3 same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:02
-	0	initializ\$5 same (null empty idle) same (all adj3 entries) same (queue adj location\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:02
-	0	initializ\$5 same (null empty idle) same (all adj3 entries) same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:02
-	178	initializ\$5 same (null empty idle) same entr\$3 same queue	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:05
-	4	(initializ\$5 adj3 queue) same ((null empty idle) with entr\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:43
-	29	(initializ\$5 with queue) same ((null empty idle) with entr\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 12:43
-	10	initializ\$5 with (queue with entr\$3) with (null idle empty)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 13:01
-	0	initializ\$5 with (queue with entr\$3) with all	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 13:01
-	157	initializ\$5 with (queue with entr\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 13:01
-	183	distributed adj shared adj memory adj system	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 18:16
-	57	CCNUMA	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 18:18
-	35	(distributed adj shared adj memory adj system) and @ad<20000720 and (arbit?r arbitration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/02 18:21
-	12	(memory adj interface) same ((plurality plural) adj3 (processor\$1 microprocessor\$1 cpu\$1)) same (shar\$3 adj (memory ram sram dram))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 09:00

-	1	(memory adj interface) same ((plurality plural) adj3 (processor\$1 microprocessor\$1 cpu\$1)) same (shar\$3 adj (memory ram sram dram)) same (arbit?r arbitration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 09:00
-	21	arbit?r adj3 (cache adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 11:23
-	316	(memory adj interface) with (cache adj memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 11:23
-	0	(memory adj interface) with (cache adj memory) with ((arbitration arbit?r) adj3 queue)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 11:24
-	0	(memory adj interface) with (cache adj memory) with ((arbitration arbit?r) with queue)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 11:24
-	1	(memory adj interface) same cache same ((arbitration arbit?r) with queue)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/03 11:51